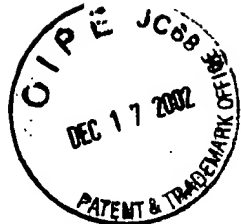


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JMS/GMB/rac
November 27, 2002



PATENT APPLICATION
Docket No.: 2789.2011-001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

6/ Declaration
Step to
3-24-03

Applicants: Ramin Farjad-Rad

Application No.: 09/862,368

Group: 2817

Filed: May 22, 2001

Examiner: Arnold M. Kinead

Confirmation No.: 8681

For: Frequency Acquisition for Data Recovery Loops

CERTIFICATE OF MAILING	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231	
on <u>12/11/02</u>	<u>Rachel Cohen</u>
Date	Signature
<u>Rachel Cohen</u>	
Typed or printed name of person signing certificate	

DECLARATION OF RAMIN FARJAD-RAD UNDER 37 C.F.R. §1.131

The Assistant Commissioner
of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Ramin Farjad-Rad of 405 Mountain Laurel Court, Mountain View, CA 94043, declare and state that:

1. I am the inventor of the above-captioned application filed on May 22, 2001, which claims the benefit of provisional Application Serial No. 60/206,191, filed on May 22, 2000.
2. A summary paper which I co-authored, entitled "A 0.3- μ m CMOS 8-Gb/s 4-0PAM Serial Link Transceiver" was published at the 1999 Symposium on VLSI Circuits, held in Kyoto, Japan between June 17 and June 19, 1999. See Exhibit A, which is a copy of this paper as published.

3. This summary paper, particularly on pages 42-43 and referring to Fig. 5, shows that I was in possession of the invention at the time the paper was published, *i.e.*, June 17, 1999. Fig. 5a illustrates a dual loop data recovery system using a data phase detector and a frequency detector, and a selector to select one of the detectors to drive a voltage controlled oscillator (VCO), as well as "loop switching decision logic" which, according to Fig. 5b comprises essentially the same circuitry as is illustrated in my patent Application, in Figs. 2 and 7, and as recited in at least independent Claims 1, 17, 32 and 34. Reduction to practice is evidenced by Fig. 7, which is a photograph of the chip die.
4. This summary paper was submitted to the Symposium by January 8, 1999, as was required for acceptance. Exhibit B is a copy of the Announcement, requiring submission by January 8, 1999. Therefore I was in possession of the invention, and the invention had been reduced to practice, at least as early as January 8, 1999.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.



Ramin Farjad-Rad



Date